REMARKS

The Examiner is thanked for the careful review of the application as set out in the outstanding office action. Reconsideration of the application is respectfully requested.

A marked up version of the changes made to the application showing the changes made is attached hereto.

In the outstanding office action, Claims 13 and 26 stand rejected under Section 112, second paragraph, as being indefinite for depending from canceled claims. Claims 27, 5, 14, 21, 28, 29; 34, 31, 35; and 33, 36 stand rejected under Section 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Claims 31, 35 have been rejected under 35 USC § 103 as being unpatentable over Meyer in view of Loo et al. ("Loo"). Claims 33 and 36 have been rejected as being unpatentable over Nakahara in view of Meyer and Loo. Claims 27, 5, 4, 21 have been rejected as being unpatentable over Loo in view of Meyer.

The rejection under Section 112, second paragraph, has been addressed by amending the dependency of Claims 13 and 26, to depend from Claims 31 and 27, respectively.

Turning now to the rejection under Section 112, first paragraph, reconsideration of the rejection is respectfully requested. The limitations identified in the office action, i.e. "selectable individually and in parallel combinations," are fully supported by applicants' specification, e.g., at 23:12 to 24:9, and FIGS. 19-20. Withdrawal of the rejection is respectfully requested.

The rejections under Section 103 are also respectfully traversed, on the grounds that a prima facie case of obviousness has not been established, and the references do not teach or suggest the claimed invention.

Claim 31 is drawn to an RF reflection phase shifter circuit, wherein the MEM switch circuit includes first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually and in parallel combinations to select different phase shift values. Meyer and Loo, alone or in combination, do not teach or suggest such a circuit.

Meyer discloses a circuit wherein either impedance Z or Z1 can be selected by the diode 12; both impedances can not be selected in parallel combinations to select an additional phase shift value. Loo is cited only as showing the use of MEM switches, and fails to supply the missing teachings.

To establish prima facie obviousness, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In regard to the consideration of claims for obviousness, it is well established that "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 165 USPQ 494, 496 (CCPA 1970). Because the applied prior art does not teach or suggest all claim limitations, a prima facie case of obviousness has not been established. The rejection of Claim 31, and of Claim 35 depending therefrom, should be withdrawn.

Claims 33, 36 stand rejected as being unpatentable over Nakahara in view of the combination of Meyer and Loo. This rejection is respectfully traversed, on the grounds that a prima facie case of obviousness has not been established, and the applied references do not teach or suggest the claimed invention.

Claim 33 is drawn to a multi-section RF phase shifter circuit, comprising:

a plurality of reflection phase shift sections connected in series to provide a discrete set of selectable phase shifts to RF signals passed through the circuit, and wherein each reflection phase shift section includes:

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports;

a switch circuit comprising a plurality of single-pole-single-throw (SPST) micro-electro-mechanical ("MEM") switches responsive to control signals, said switch circuit arranged to select one of a plurality of discrete phase shift values introduced by the phase shifter circuit to RF signals passed between the first and second RF ports;

said MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually and in parallel combinations to select different phase shift values.

The applied references do not teach or suggest a MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually and in parallel combinations to select different phase shift values. Nakahara does not disclose the selection of parallel combinations of terminating susceptances, but only selection of one reactance leg or the other, or neither reactance leg. As discussed above, Meyer and Loo do not disclose this feature either.

In order to achieve the same number of possible phase states provided by the phase shifter of Claims 33 and 35, Nakahara would need to add additional phase shifter stages connected in series, with a consequent increase in cost, size and loss.

Claims 27, 5, 14 and 21 stand rejected as being unpatentable over Loo and Meyer taken together. Claim 27 is drawn to an array including an array of reflection phase shifters, including a plurality of micro-electro-mechanical ("MEM") switches responsive to said control signals to select one of a discrete number of phase shift settings for the respective phase shifter, a coupler device having first and second RF I/O ports, and in-phase and quadrature ports, and first and second reactance circuits respectively coupled to the in-phase and quadrature ports by first and second MEM switch circuits, said first and second reactance circuits each comprising a plurality of susceptances connected in parallel for terminating said in-phase or quadrature port, and wherein first and second MEM switch circuits select at least one of said plurality of susceptances connected in parallel for each of said first and second reactance circuits to select a phase shift setting, and wherein said plurality of susceptances can be selected individually and in parallel combinations.

Loo and Meyer, taken alone or in combination, do not disclose or suggest a reflection phase shifter having first and second reactance circuits as recited in Claim 27. Selecting individually and in parallel combinations of terminating susceptances is not taught or suggested by the applied art. The capability of selecting individual and parallel combinations of terminating susceptances increases the number of phase states for the phase shifter. Meyer does not disclose the selection of parallel combinations of terminating susceptances, but only selection of one reactance leg or the other. Loo does not disclose this feature either.

In order to achieve the same number of possible phase states provided by the phase shifter of Claim 27, Meyer would need to add additional phase shifter stages connected in series, with a consequent increase in cost, size and loss.

Conclusion

The outstanding objections and rejections have been addressed, and the application is now in condition for allowance. Such favorable reconsideration is solicited.

Respectfully submitted,

Registration No. 30,021

Leonard A. Alkov, Attorney for Applicants

Tel. No. 310.647.2577
Fax No. 310.647.2616

Raytheon Company
P.O. Box 902 (E1/E150)
El Segundo, CA 90245-0902

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

13. (Amended) The circuit of Claim [12] 31, wherein said first and second MEM switch circuits provide MPMT switching functions.

26. (Amended) The array of Claim [25] 27 wherein said single MEM switch provides said reference signal path.